ABSTRACT OF THE DISCLOSURE

A wafer level testing and bumping process is provided. A plurality of test pads serving as testing point for testing and analyzing the circuits within the wafer is formed on the active surface of the wafer. The test pads are electrically connected to the flip-chip bonding pads respectively. The test pads are positioned on the peripheral section of the active surface. The tip of probe pins hanging from a cantilever probe card touches the test pads so that the wafer can be tested through the probe pins to obtain some test results. Whether to cut a particular fuse line underneath a fuse window by aiming a laser beam at the fuse window can be determined according to the test results. Finally, a passivation layer and bumps are formed on the active surface of the wafer and then the wafer is cut to form a plurality of single chips ready for performing subsequent packing processes.